Professional H.265/HEVC Encoder LSI Toward High-Quality 4K/8K Broadcast Infrastructure

Hiroe Iwasaki, Takayuki Onishi, Ken Nakamura, Koyo Nitta, Takashi Sano, Yukikuni Nishida, Kazuya Yokohari, Jia Su, Naoki Ono, Ritsu Kusaba, Atsushi Sagata, Mitsuo Ikeda, and Atsushi Shimizu

NTT Media Intelligence Laboratories

NTT Corporation

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History of NTT's Video CODEC LSIs

Analog *Digital* → SDTV *HDTV* → MPEG2 *H.264* → HDTV *UHDTV* / H.264 *H.265*

Encoder PCI Board

Portable HDTV Encoder (ICCE2001)

Encoder PC Card (ICCE2000)

ENC-C/-M ('95) (HotChips7)

SuperENC ('98) (HotChips10)

SuperENCII('00)

VASA ('02) (HotChips14)

NHK/NTT-COM Board

HDTV MPEG-2 Encoder

HDTV MPEG-2 Decoder

ISIL-II ('07) (CoolChips X)

ISIL('02) (CICC2003)

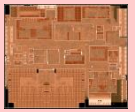
MPEG-2/H.264 Transcoder

HDTV H.264 Decoder

HDTV H.264 Encoder

SARA('07) (HotChips19)

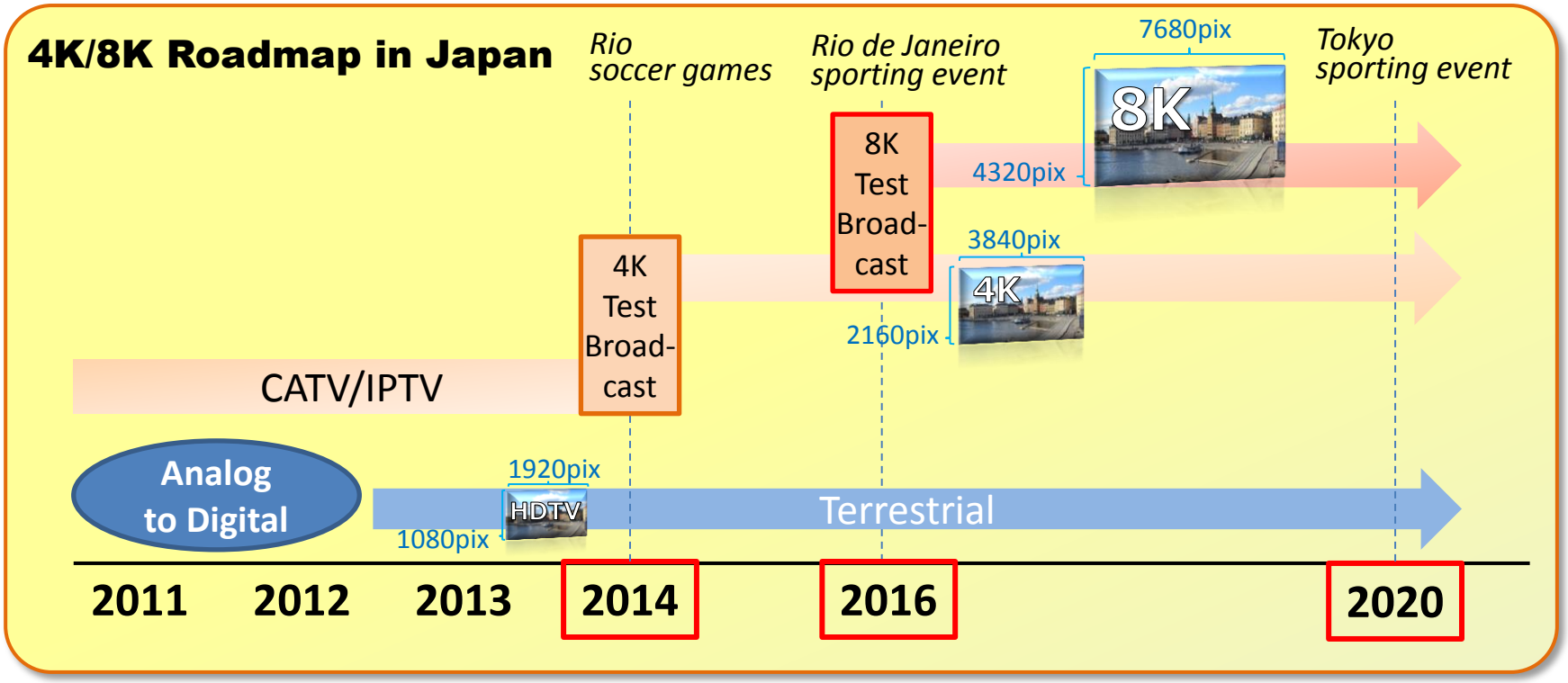
SARA/D ('08) (CoolChips XI)



NARA('15) (Symp.VLSI2015)

Roadmaps toward 4K/8K UHDTV

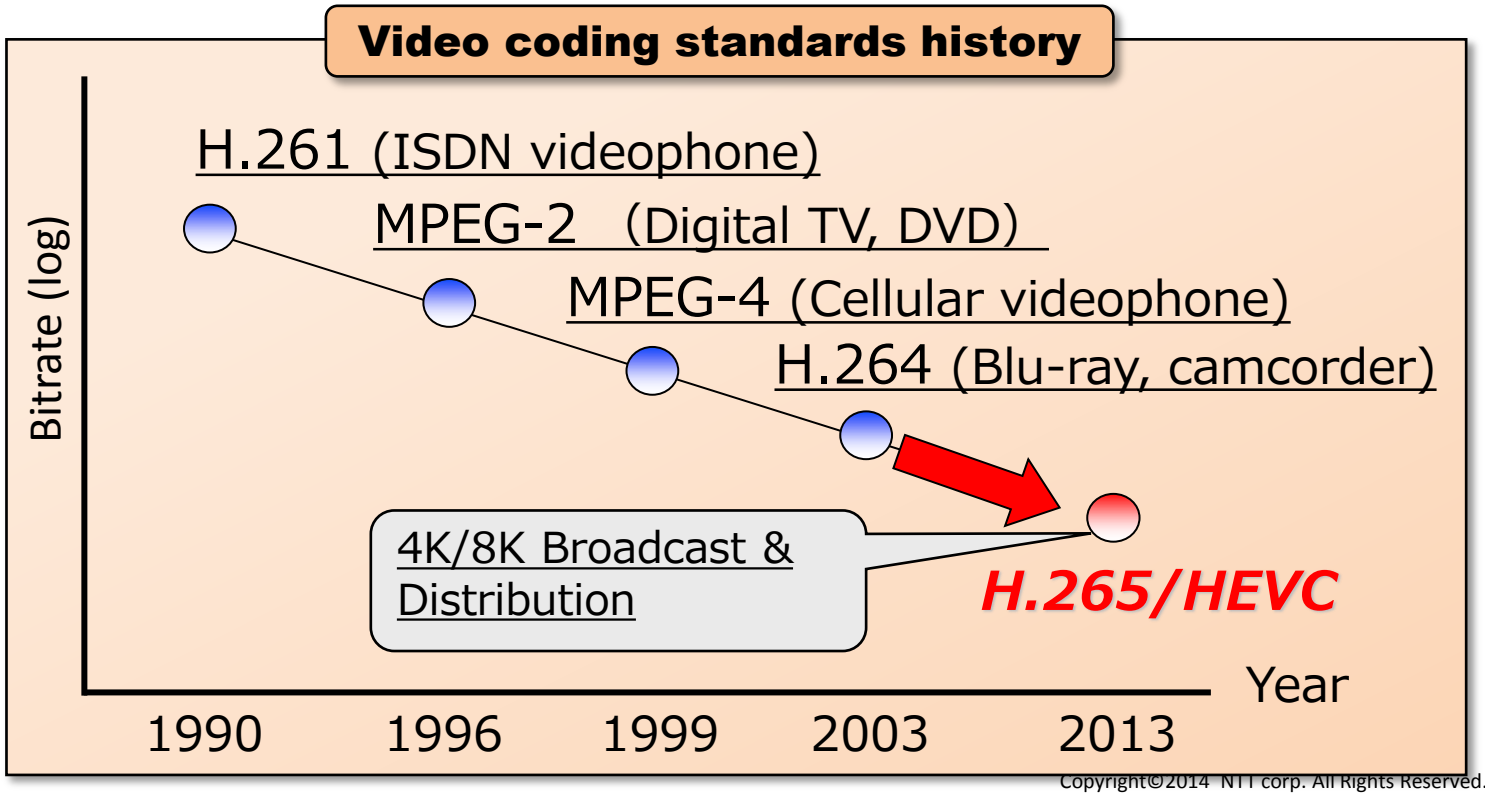
- 4K test broadcast over satellite in 2014, 8K in 2016
- 4K/8K broadcast TV programs in 2020



Reference: Interim Report of 4K/8K Roadmap Follow-up Meeting (MIC, Japan)

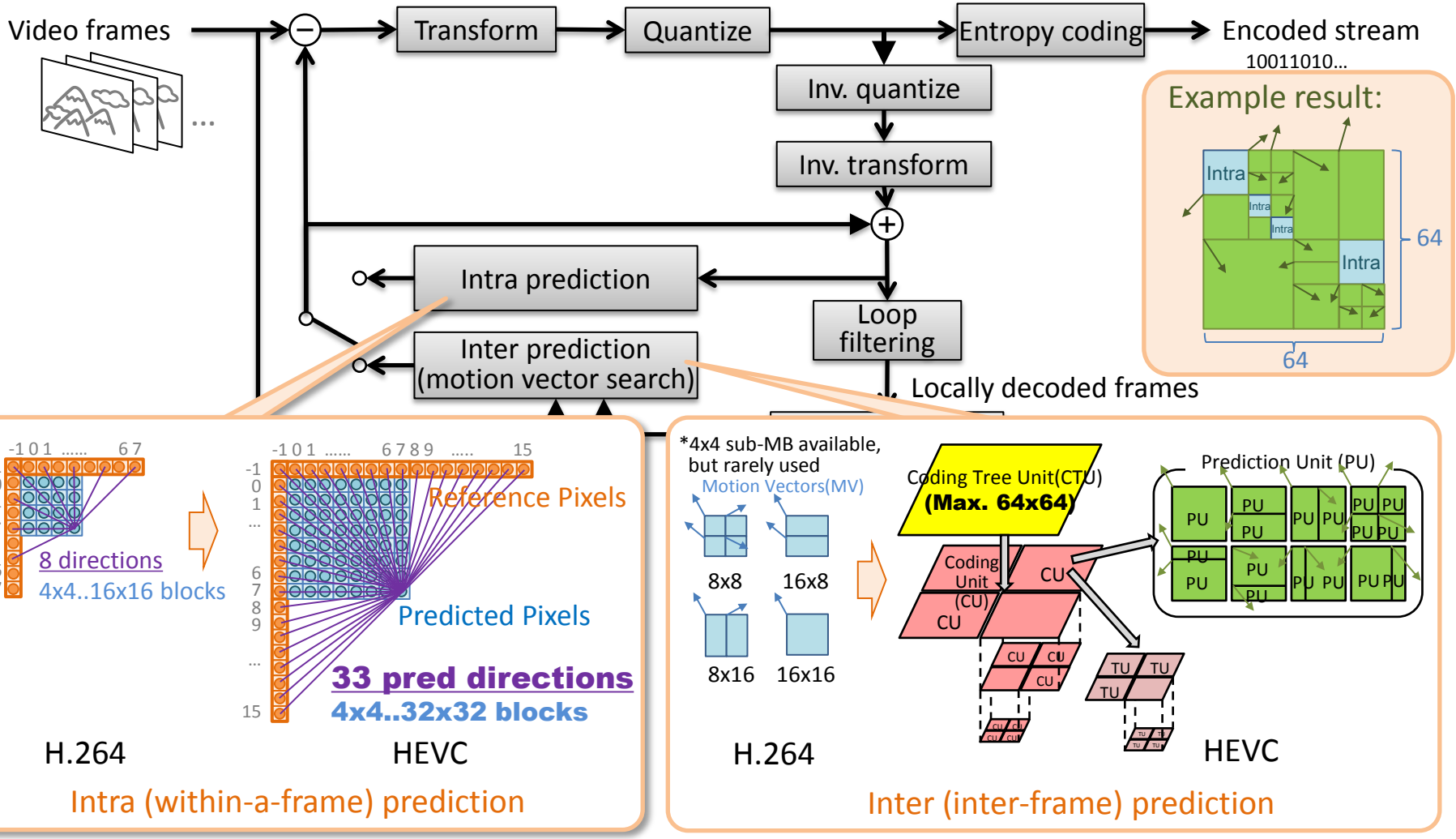
HEVC – High Efficiency Video Coding

- The latest video coding standard (Jan. 2013, Range extensions Apr. 2014)
- Achieves half bit rate compared to H.264, 1/4 to MPEG-2, key technology for 4K/8K



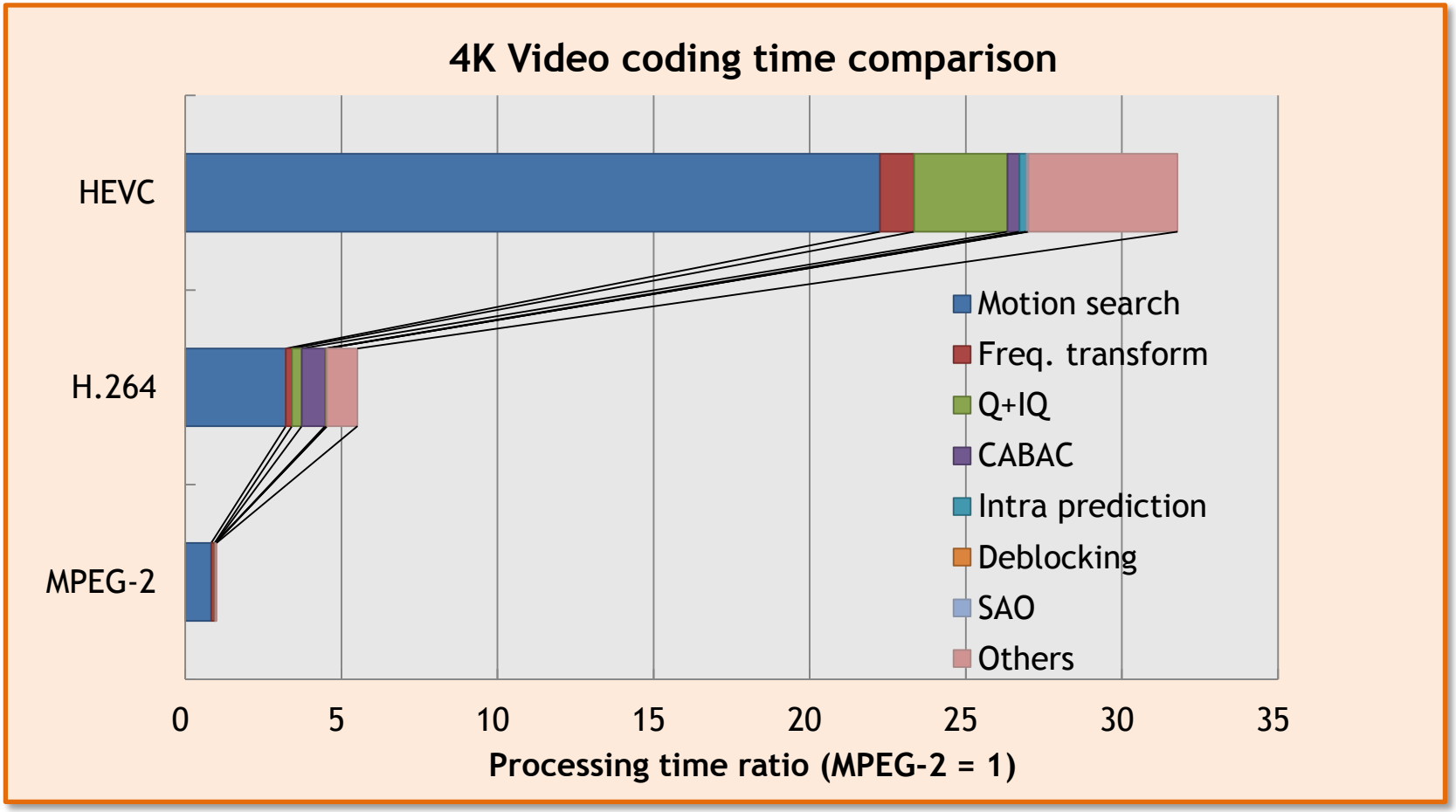
What is HEVC?

- Existing encoding flows, but “adaptive and exhaustive” combination of prediction tools



HEVC Encoding Complexity

- About 30x of MPEG-2, 5x of H.264



Reference software: MPEG-2_MSSG H.264_JM18.5 HEVC_HM12.1

Requirements for 4K/8K broadcasting

Innovative R&D by NTT

- High-quality 4K/8K broadcast infrastructure in 2020
- The latest video coding standard for high-compression
- Color robustness against tandem encoding for contribution
- High bitrate up to 600Mbps for contribution

NARA: Professional H.265/HEVC encoder LSI toward high-quality 4K/8K broadcast infrastructure

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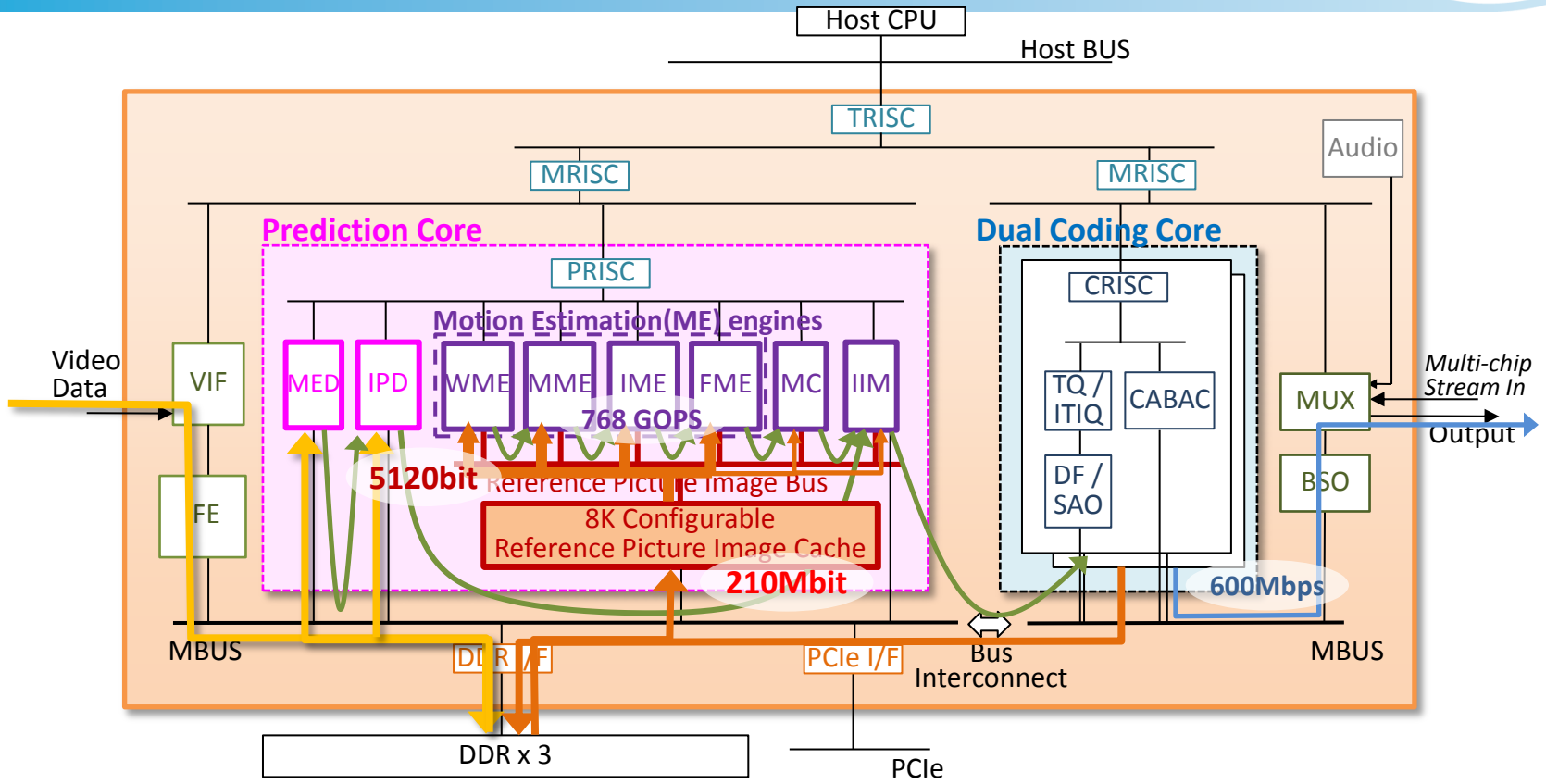
NARA Block diagram

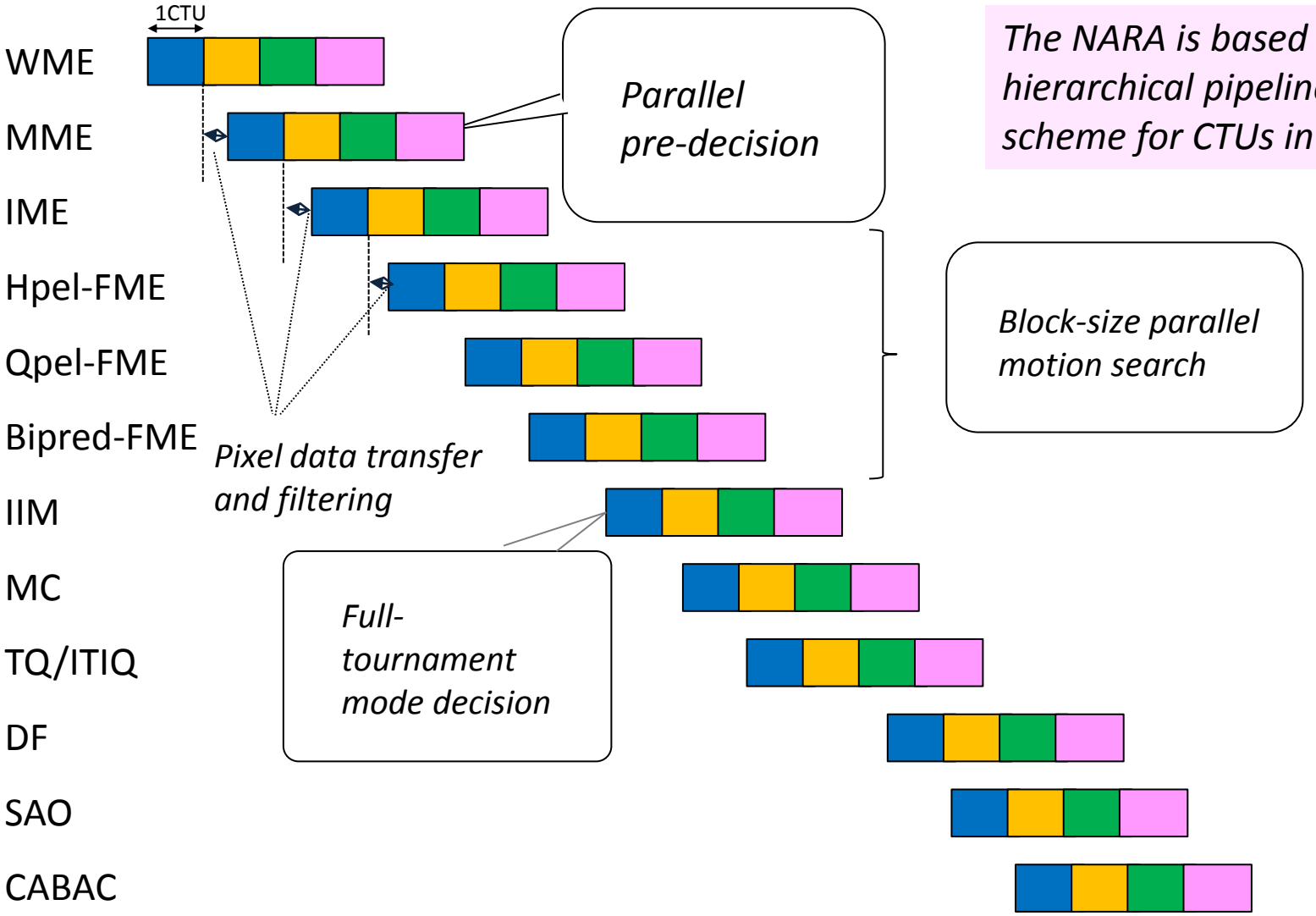


VIF: Video Interface
IFE: Image Feature Extraction
MED: Multi-block-size Edge Detector
IPD: Intra Prediction
WME: Wide-range Motion Estimation
MME: Multi-Block-Size Motion Estimation
IME: Integer pixel Motion Estimation
FME: Fractional pixel Motion Estimation

MC: Motion Compensation
IIM: Intra-Inter Mode Decision
MBUS: Memory BUS
TQ: Transform and Quantization
ITIQ: Inverse Transform and Quantization
DF: Deblocking Filter
SAO: Sample Adaptive Offset filtering

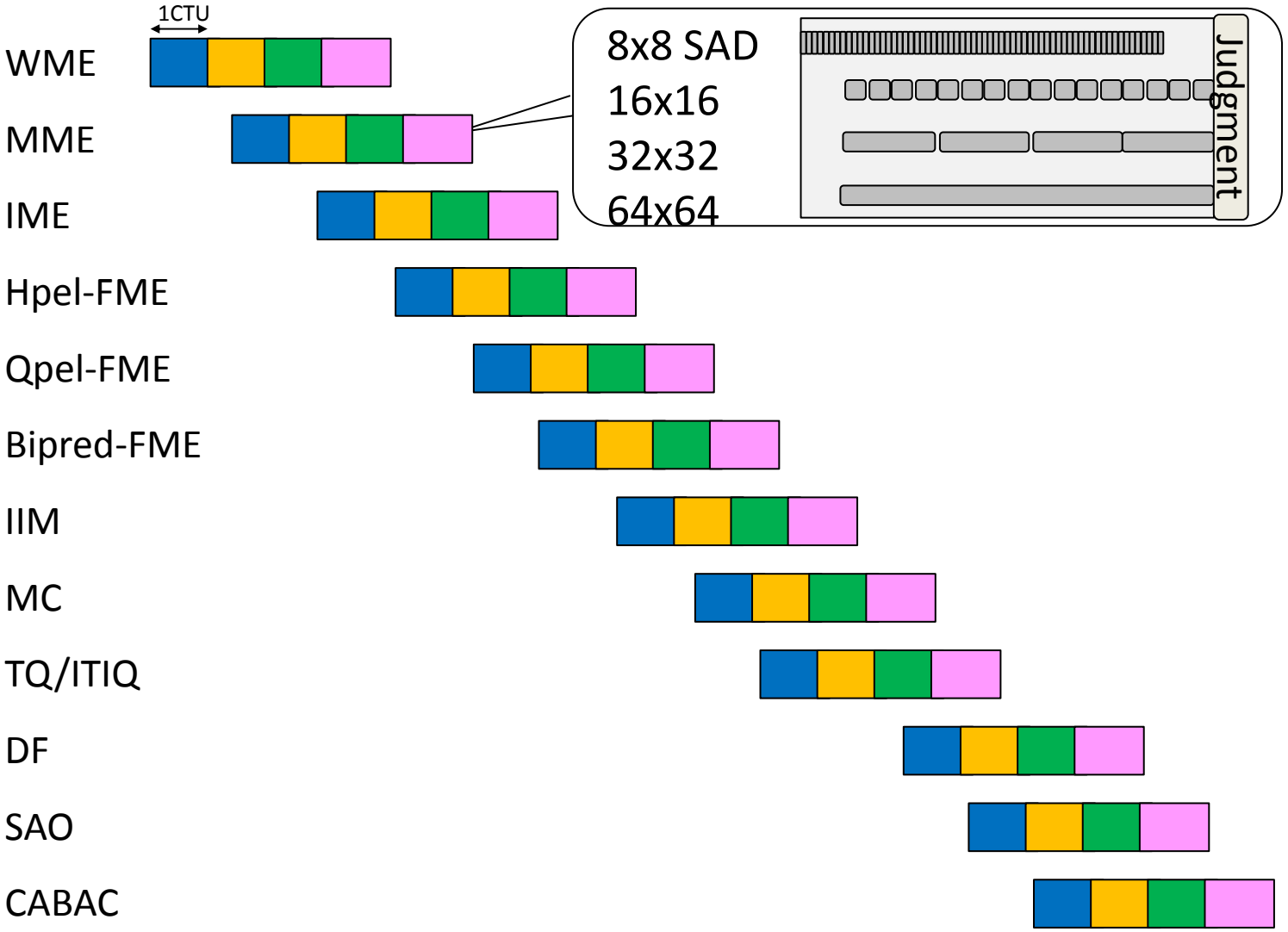
BSO: Bit Stream Out
MUX: Multiplexer
PRISC: Prediction Core RISC
CRISC: Coding Core RISC
MRISC: Middle-level RISC
TRISC: Top-level RISC

NARA Pipeline Scheme



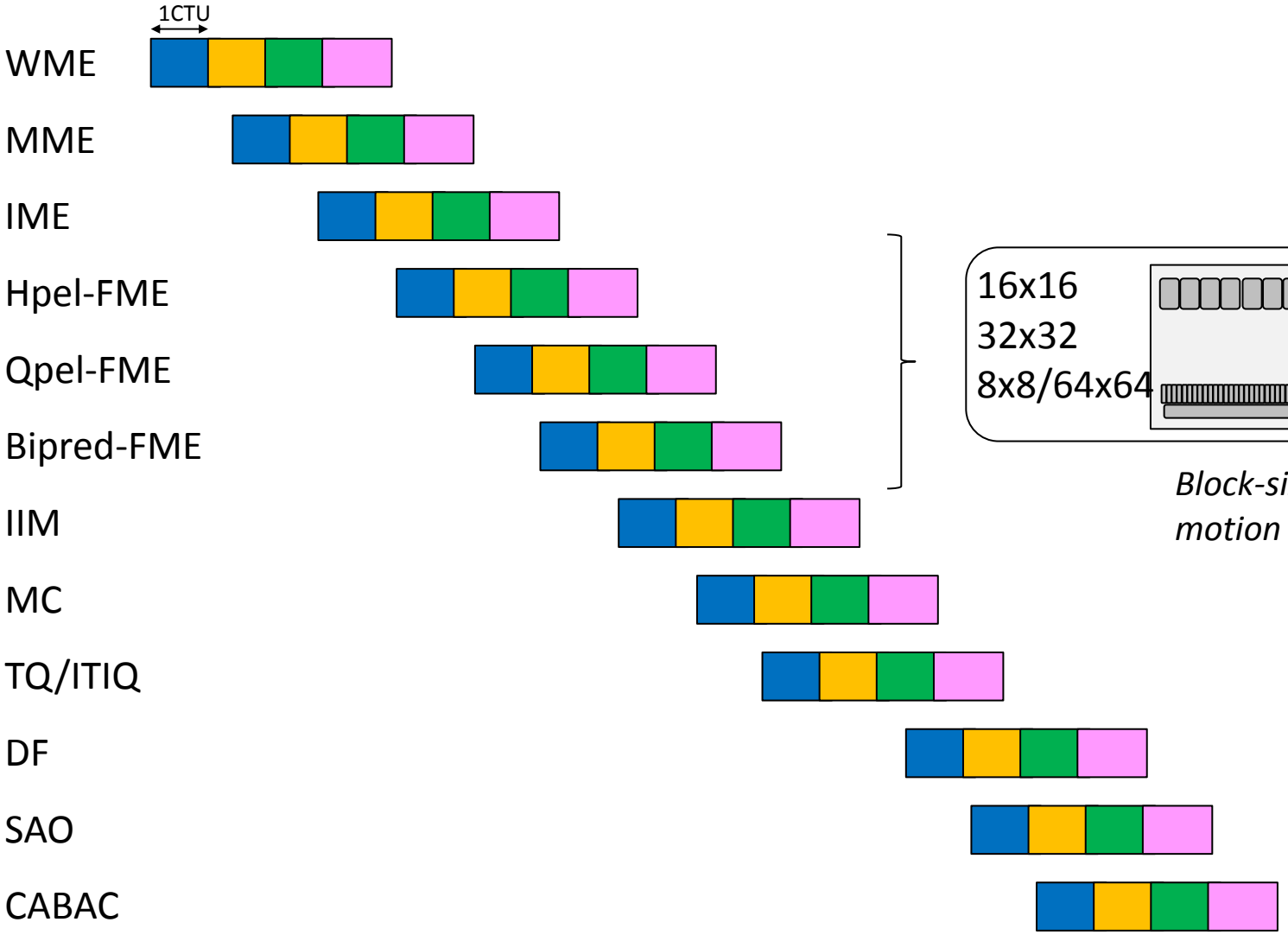
The NARA is based on hierarchical pipeline scheme for CTUs in HEVC

Parallel pre-decision in MME



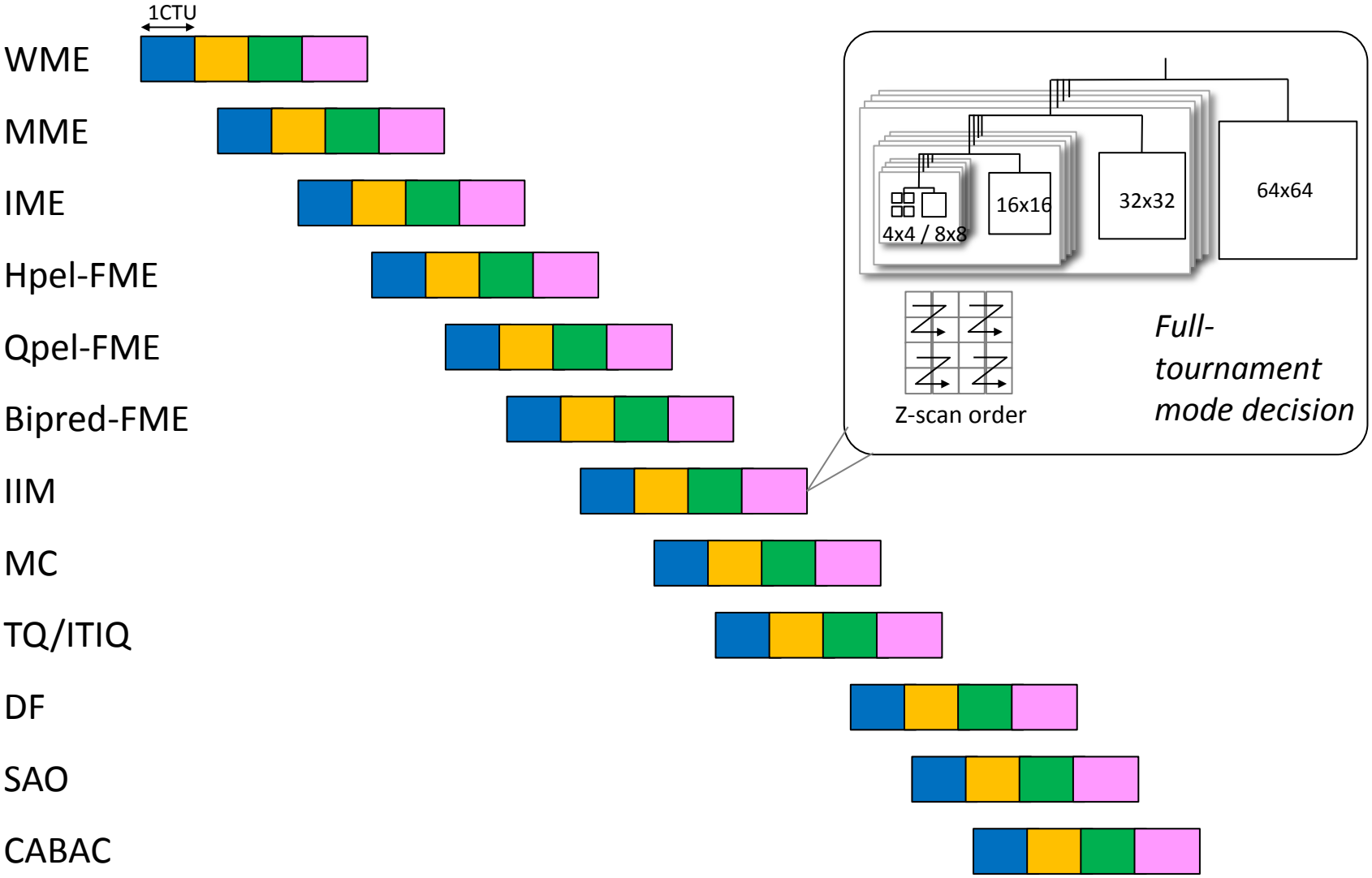
Parallel pre-decision

Block-size parallel motion search in FME

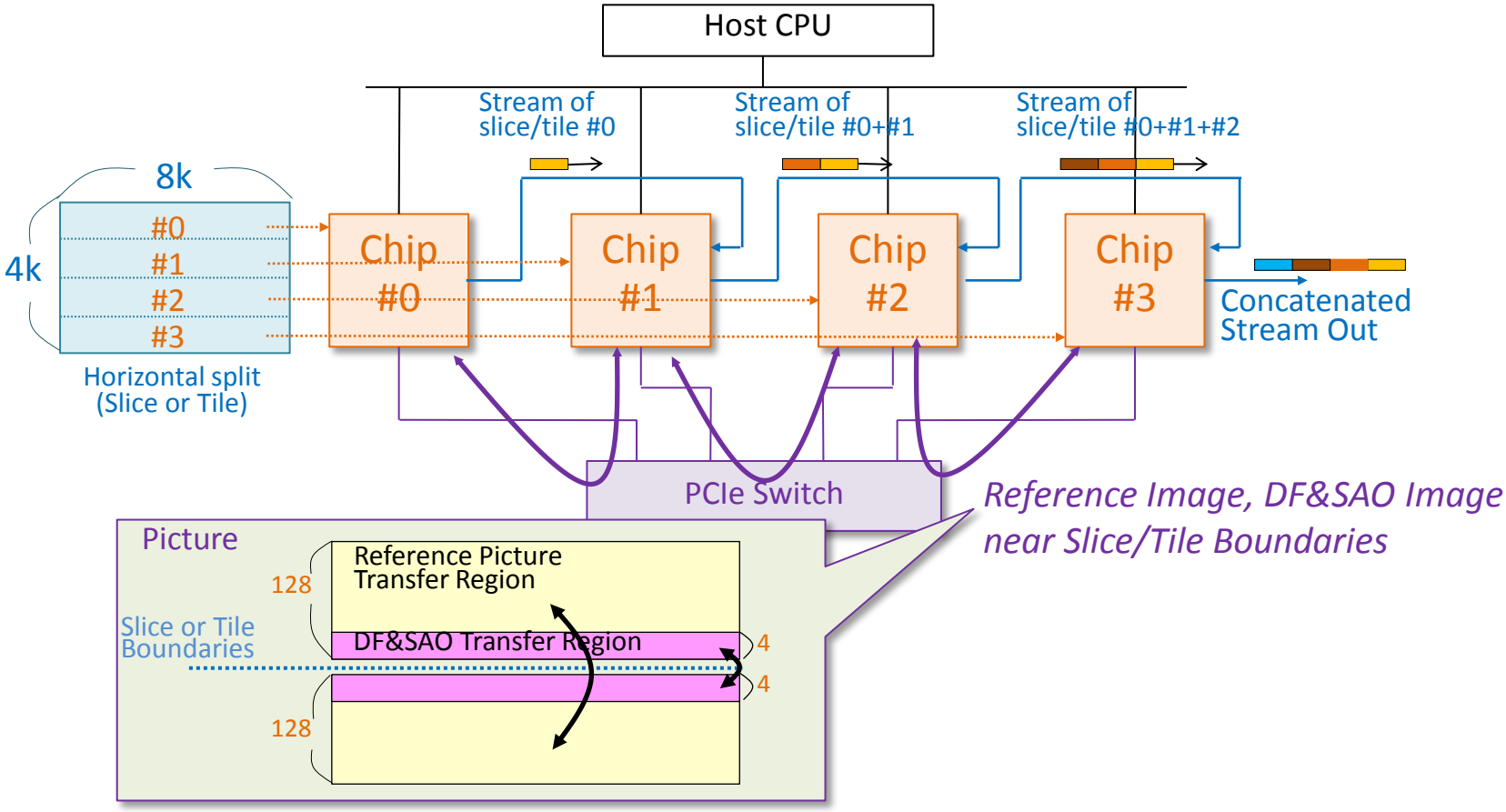


Block-size parallel motion search

Full-tournament mode decision in IIM

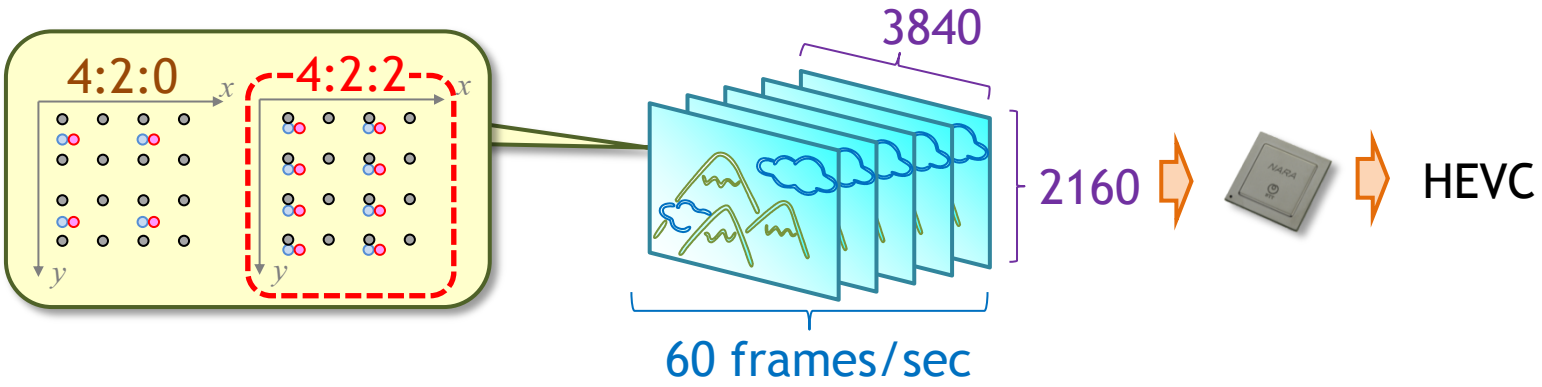


Multi-chip Configuration

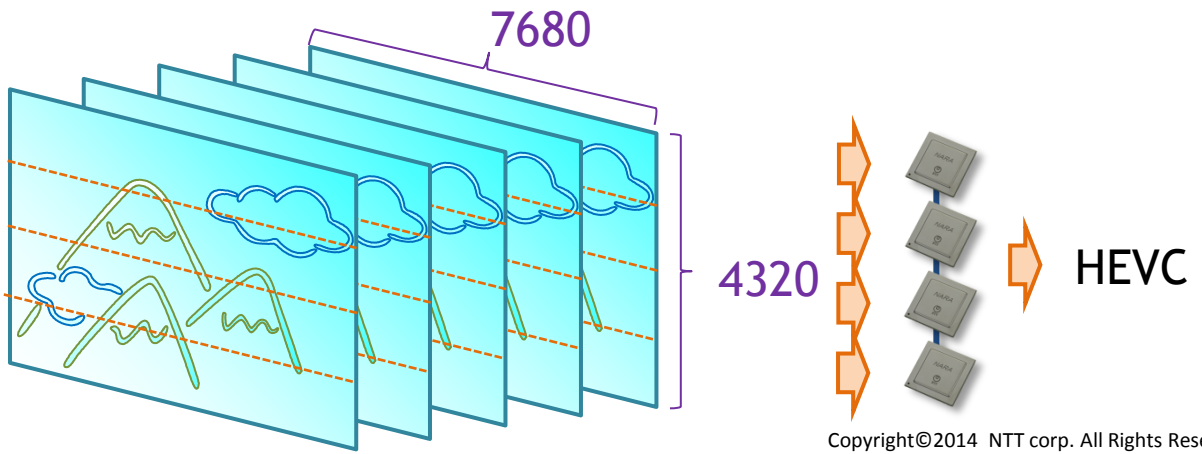


NARA Configurations

- Capability
  - Single-chip processing up to 4K 60fps 4:2:2



  - Multi-chip scalability up to 8K 60fps



NARA Key Features and Functions

Innovative R&D by NTT

Single-chip configurations:

- Complicated HEVC processing is mapped to a hierarchical pipeline scheme based on coding tree units(CTUs).
- The hierarchical pipeline achieves a wide-range motion estimation with ±3847.75 x ±1926.75 search range and an optimized HEVC's high-precision prediction mode decision.
- 4k/60p 4:2:2 real-time encoding with ultra-low delay for field pickup units (FPUs), high bitrate up to 600Mbps for contribution, multi-channel encoding for cloud systems, and multi-standard encoding for allowing a smooth migration.

Multi-chip configurations:

- The LSIs can be utilized to encode ultra-high definition TV beyond 4K with motion estimation and loop filtering across split boundaries when each chip encoders a partitioned frame.
- It is suitable for HEVC-based tandem encoding with 4:2:2 for keeping good color information and two-pass encoding for higher compression of final distribution.

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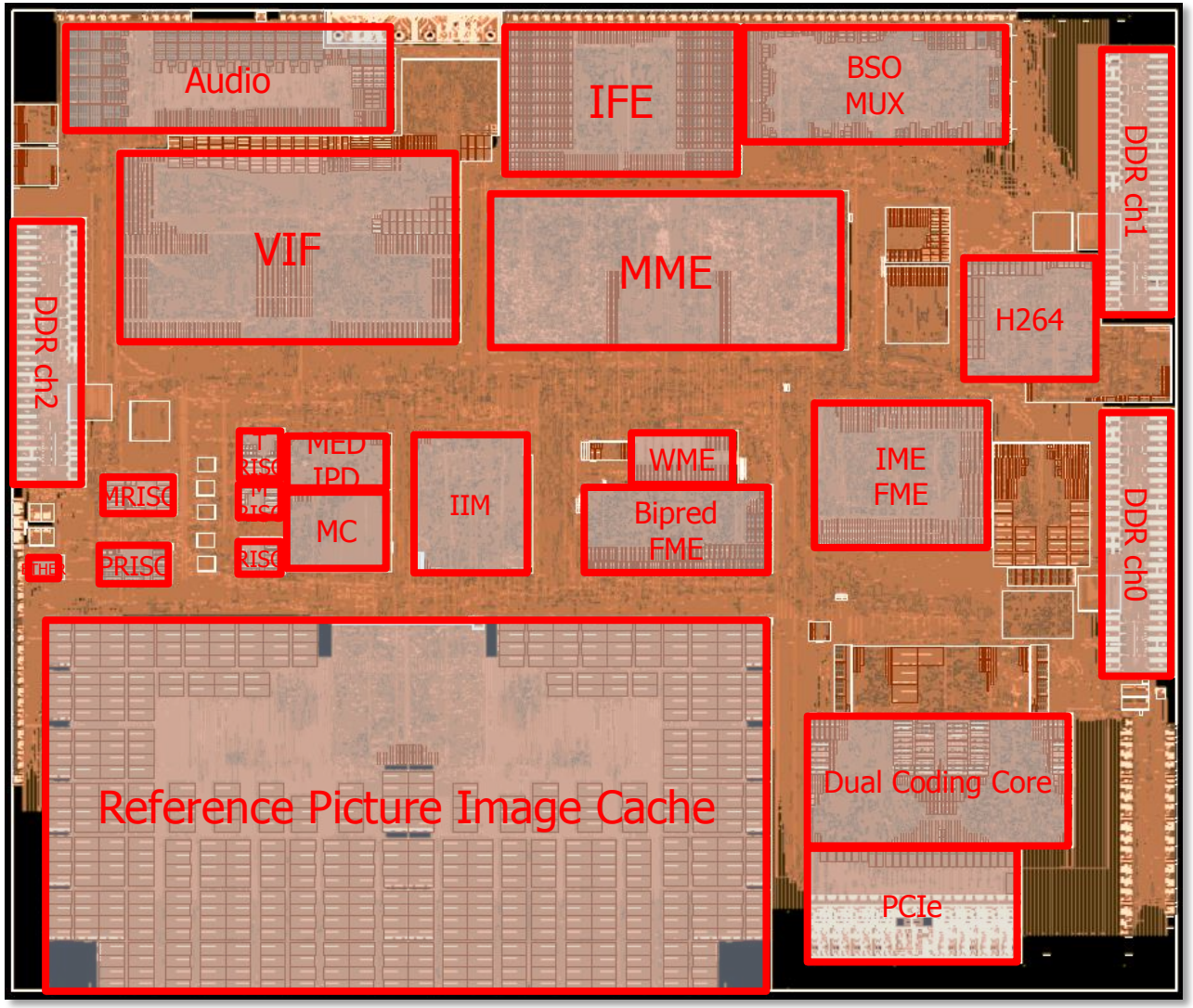
NARA Chip Implementation



NARA Physical Features

Technology	28nm CMOS
Number of transistors	83M gates
Clock frequency	Max 600MHz
Supply voltage	Core: 0.9V IO: 1.8/3.3V DDR3: 1.5V PCIe and 3G-SDI: 0.9/1.8V
Power consumption	About 15.0W
Package	1152 pin FCBGA(35mm■)
External memories	DDR3

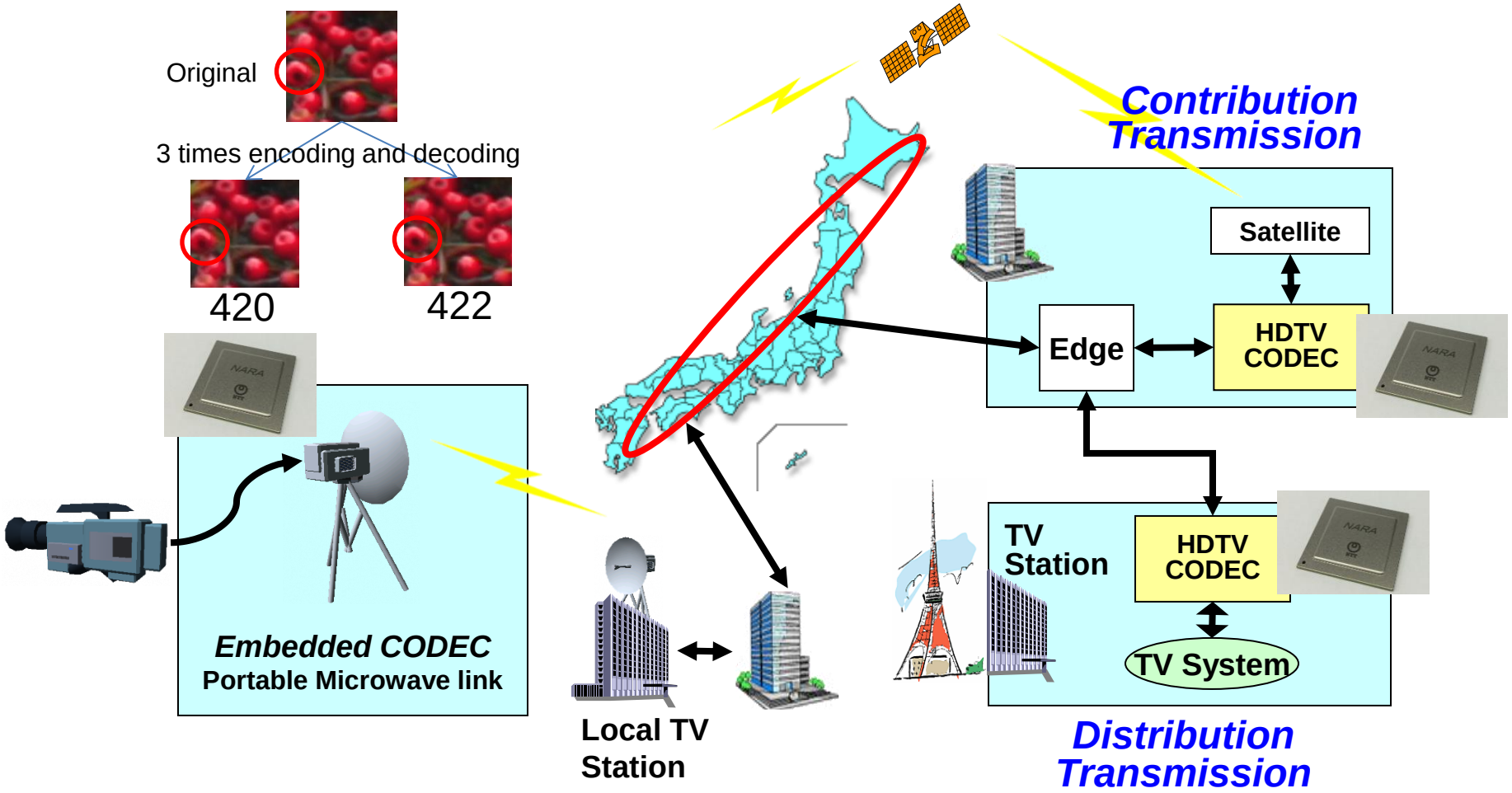
NARA Functional Features

Video	Profile	H.265/HEVC Main, Main10, 4:2:2 10 H.264/AVC Base, Main, Main10, High422
	Motion search range	-3847.75/+3847.75(H) -1926.75/+1926.75(V)
	Resolution and video rate	Single-chip: 4096x2160 at up to 60 frames per second Multi-chip: 7860x4320 at up to 60 frames per second
Others	Audio: Serial I/F x 2 Port Stream Out: Parallel x 1 /Serial x 4 PCIe: Gen.2 x 8 Lane Ethernet: 1000/100/10 Mbps with MAC Others: User PES input, STC input/output	

Target Applications

Innovative R&D by NTT

Digital TV Broadcasting Network Service



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Target Applications

- Museums, galleries

- Digital cinema
  (Projectors, screens)
- Box office sales

- Conferencing systems/services
- Projectors

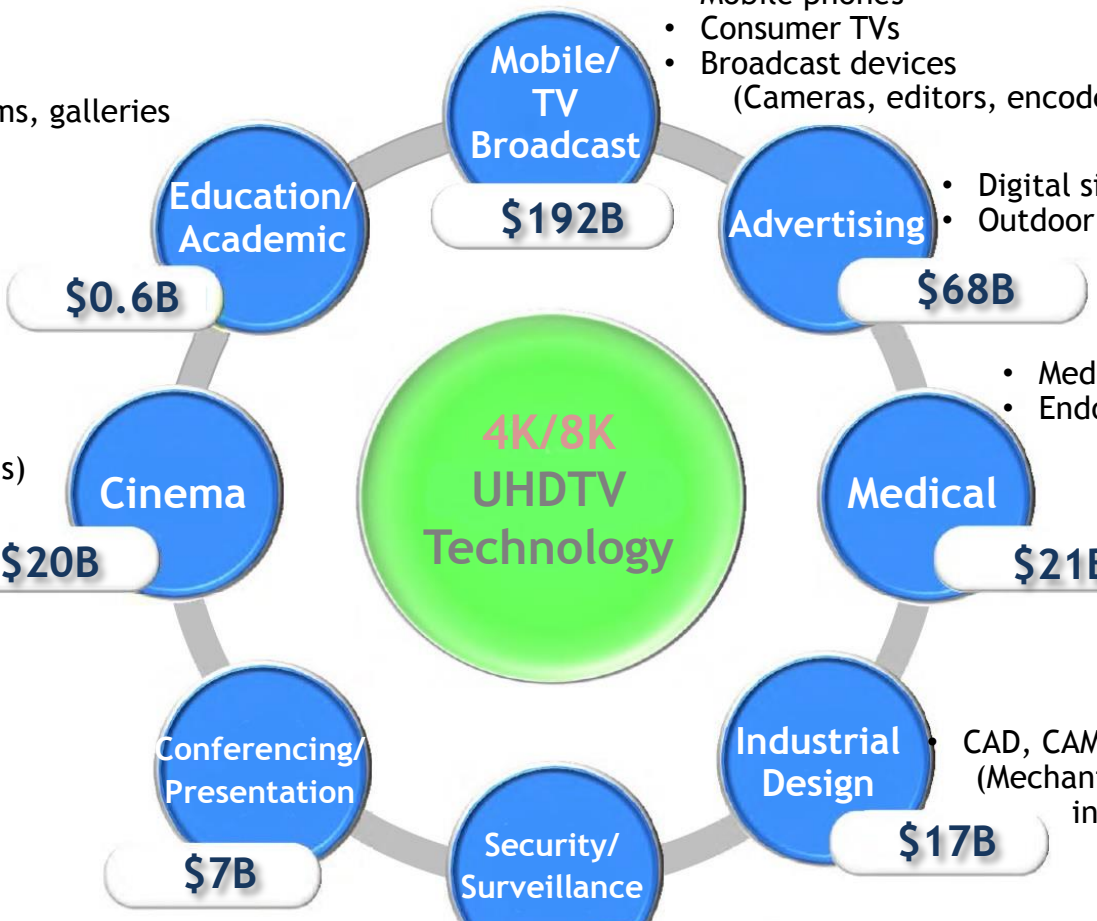
- Security (surveillance) cameras
- Industrial camera sensors

- CAD, CAM, CG
  (Mechanical, automotive, industrial designs)

- Medical monitors
- Endoscopic systems

- Digital signage
- Outdoor display LEDs

- Mobile phones
- Consumer TVs
- Broadcast devices
  (Cameras, editors, encoders)



Reference: Interim Report of 4K/8K Roadmap Follow-up Meeting (MIC, Japan) *1USD= 120JPY

Conclusions

- A single-chip 4K 60fps 4:2:2 HEVC video encoder LSI has been developed, scalable to 8K 60fps
- 8K scalability is ready with inter-chip connectivity and parallel processing functions
- NARA Main Architecture has hierarchical pipeline scheme for CTUs

NARA is a key LSI for Professional H.265/HEVC encoder LSI toward high-quality 4K/8K broadcast infrastructure